

Analysis of Planar Circuits with a Combined 3D FDTD-Time Domain Modal Expansion Method

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Abstract

A method combining the conventional 3D FDTD algorithm with the time domain modal expansion has been applied to the analysis of planar circuits enclosed within metallic packages. This method allows for the reduction of the 3D FDTD computational domain to a restricted region close to the planar circuit. This technique has been applied to two different structures: a microstrip and a CPW discontinuity. The results show a significant improvement of the computational efficiency without any appreciable degradation of the accuracy.

1. Introduction

Since its appearance in 1966 [1], the Finite Difference Time Domain (FDTD) method has been extensively applied to the analysis and characterization of discontinuities in planar structures. First, Koike et al. analyzed a microstrip gap [2], then, Zhang et al. [3] characterized a microstrip open circuit, later, Liang et al. adopted the FDTD method to characterize Coplanar Waveguide (CPW) discontinuities [4]. Later the method has been used to simulate many kinds of planar circuits and their interaction with the package and interconnects [5-9].

Recently, a new technique has been proposed to improve the efficiency of the original FDTD method to treat waveguide discontinuity problems [10-14]. This method is based on the combination of the 3D FDTD with the time domain eigenfunction expansion of the electromagnetic field. Mrozowski et al. proposed to adopt this technique also for the 2D analysis of Microwave Monolithic Integrated Circuits (MMIC) [15]. In the present contribution, the method [14] has been adapted to the simulation of a three dimensional planar structures such as CPW and microstrip discontinuities. The method has been compared with experiments and with the conventional 3D FDTD method. The results obtained show a significant improvement of the original computational efficiency, without any appreciable degradation of the accuracy.

2. The Method

A detailed description of the method is given in [14]. Here the method is briefly outlined. Consider a planar

circuit enclosed in a metallic box, Fig. 1.

Along the direction perpendicular to the metallization plane (z direction of Fig. 1) the structure is seen as the cascade of regular and irregular regions. The former (zones A and C in Fig. 1) are the uniform waveguides corresponding to the empty parts of the metallic box above and below the planar circuit. The latter (zone B in Fig. 1) includes the feeding coaxial connectors and the planar circuit itself. The Electromagnetic (EM) field into the irregular region is evaluated by using the conventional 3D FDTD algorithm and a unidirectional graded mesh [16]. The uniform regions are modeled, in time domain, by means of transmission lines representing the waveguide modes. Each modal voltage (V_n in formula 1) satisfies the following wave equation:

$$\frac{\partial^2 V_n}{\partial z^2} - \frac{1}{c_0^2} \frac{\partial^2 V_n}{\partial t^2} - k_{cn}^2 V_n = 0 \quad (1)$$

where k_{cn} is the eigenvalue of the waveguide mode of order n . This equation is solved adopting a 1D centered difference scheme, thus leading to:

$$V_{n,k}^{t+1} = \frac{c_0^2 \Delta t^2}{\Delta z^2} (V_{n,k+1}^t - 2V_{n,k}^t + V_{n,k-1}^t) - c_0^2 \Delta t^2 k_{cn}^2 V_{n,k}^t + 2V_{n,k}^t - V_{n,k}^{t-1} \quad (2)$$

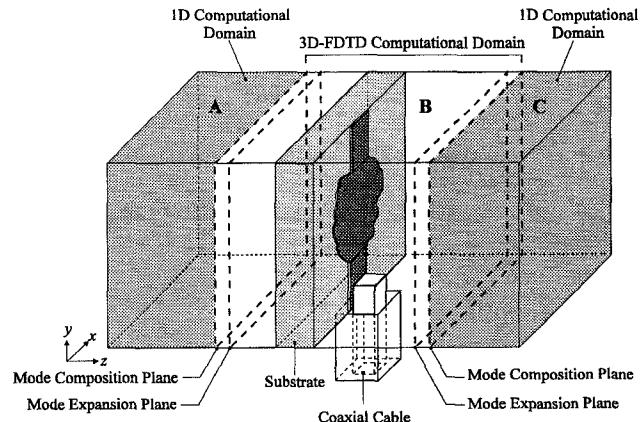


Fig. 1. Arbitrary planar circuit including feeding coaxial connector. The circuit is enclosed within a metallic box.

In this manner the complexity of the problem is reduced from 3D to 1D, thus resulting in a computational saving. Since the algorithm is marching in time, at each step the transmission lines are interfaced with the 3D FDTD computational domain (Fig. 1).

First, the modal voltages are computed by taking the scalar product of the waveguide eigenvectors with the transverse electric field over the mode expansion plane (Fig. 1).

Second, the transverse electric field over the mode composition plane in (Fig. 1) is evaluated as a superposition of waveguide modes. These two steps provide all boundary conditions for the 3D domain. For the 1D domain the modal lines are to be shorted.

3. Description of the structures

The method has been applied to two different planar circuits using microstrip and CPW technologies. The structures analyzed consist of a microstrip via-hole and a double step in coplanar waveguide. Both include the package and the feeding coaxial lines. The feeding lines have been approximated as $50\ \Omega$ coaxial lines with square cross section (not shown in figures).

Fig. 2 shows the sketch of the microstrip via-hole. For simplicity, the section of the via-hole has been approximated with a square shape [7, 17].

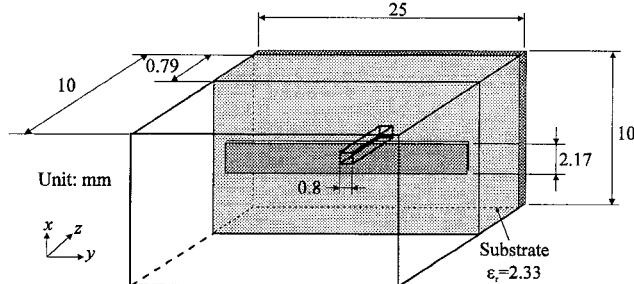


Fig. 2. Sketch of the microstrip via-hole.

The microstrip circuit has been enclosed into a package, the dimension being $10 \times 25 \times 10$ mm. This package exhibits a first resonant frequency around 15 GHz [7]. The structure has been excited by a gaussian pulse with the 95% of the power within the band 0-14 GHz. The exciting field pattern, (fundamental mode) has been calculated numerically by performing an FDTD simulation of the uniform coaxial line [5]. In order to allow for an easy separation between the reflected and the incident pulse, a length of 32 mm has been adopted for the input cable. For the output cable, only 10 mm has been used. This length is sufficient for the higher order modes, excited at the microstrip-connector transition, to vanish. The entire structure has been simulated using a variable mesh [16, 18] of $25 \times 81 \times 32$ cells.

Fig. 3 shows the sketch of the CPW double step. In this case the package has a dimension of $3.1 \times 30 \times 17.1$ mm.

the feeding coaxial lines are 50 and 10 mm long respectively and the entire structure has been discretized with $31 \times 110 \times 41$ cells. The 95% of the power of the exciting pulse is within the band 0-8 GHz.

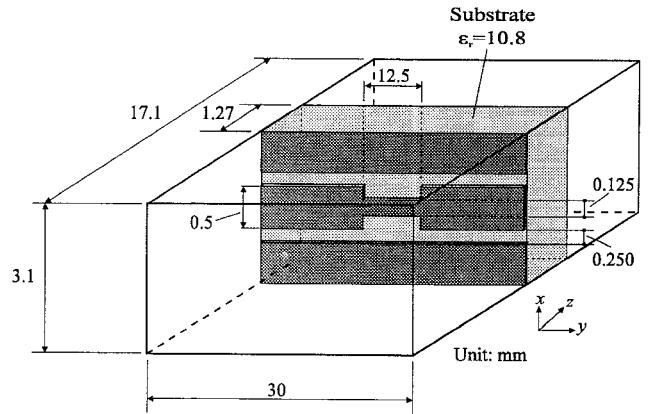


Fig. 3. Sketch of coplanar waveguide double step.

4. Results

The combined method requires the precomputation of the correct number of modes necessary for the description of the EM field at the interface planes. To evaluate this parameter we have taken into account all the propagating modes plus the evanescent modes whose magnitude is reduced by less than 10 times. The number of modes stated by this conservative criterion can be often reduced when information about the field scattered by the discontinuity is available [13]. In order to simulate the via hole, 10 modes are sufficient. Table 1 summarizes the dimensions, the computing time and the speed-up factor with respect to the conventional FDTD, obtained for this simulation.

In this case, the mesh has been reduced by about a factor 2, and, since the number of modes is quite low, the computational costs of the 1D-3D interface and of the 1D field evaluation is negligible. This is pointed out by Table 1.

MICROSTRIP VIA-HOLE				
Method	Dimensions $N_x \times N_y \times N_z$	Number of Modes	Time [sec]	Speed-up
FDTD	$25 \times 81 \times 32$	****	2540	****
FDTD + Modes	$25 \times 81 \times 17$	10	1243	2.06

Table 1. CPU time (HP 735 WS) and Speed-up factors for the microstrip via-hole.

Table 2 summarizes the results obtained simulating the second structure. In this case the reduction of the mesh is only about one fourth. Moreover, a higher number of modes and two interface regions were required.

Fig. 4 shows the insertion loss of the via hole over the whole operating frequency range of the package. The agreement between the combined approach and the full 3D

FDTD method is less than ± 0.5 dB of error, thus proving the validity of the method adopted.

COPLANAR WAVEGUIDE STEP				
Method	Dimensions $N_x \times N_y \times N_z$	Number of Modes	Time [sec]	Speed-up
FDTD	31*110*41	****	9768	****
FDTD + Modes	31*110*30	28	8262	1.18
FDTD + Modes	31*110*30	16	7491	1.30

Table 2. CPU time (HP 735 WS) and Speed-up factors for the CPW step.

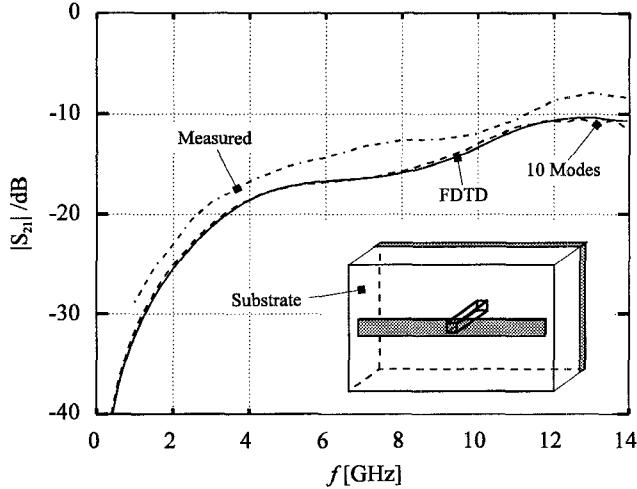


Fig. 4. Theoretical and experimental results for the $|S_{21}|$ of the microstrip via-hole.

The slight underestimation of the insertion loss with respect to the measurement has to be ascribed mainly to lossless structure assumption.

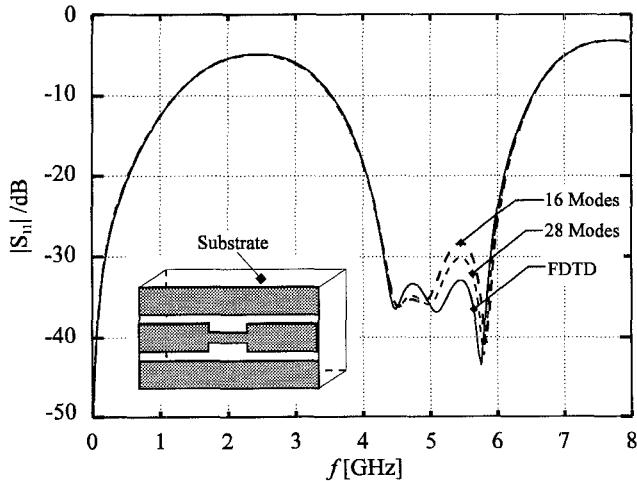


Fig. 5 $|S_{11}|$ of the CPW step. Comparison among conventional FDTD and FDTD+Modal expansion.

Fig. 5, shows the results obtained for the CPW double step. In this case, 16 and 28 modes have been adopted to evaluate the EM field at the interface planes.

All simulations coincide over most of the frequency spectrum, except within the notch. Note, however, that, increasing the number of modes leads to the convergence of the results to the 3D FDTD case.

4. Conclusions

A method combining 3D FDTD with the time domain modal expansion of the EM field has been successfully applied to the simulation of a microstrip via hole and a CPW double step. The analyses have taken simultaneously into account for the influence of the package and interconnections. The obtained results demonstrate an improvement of the computational efficiency with respect to the conventional 3D FDTD approach. Computational cost reduction by a factor 1.18 (CPW double step) and 2.06 (microstrip via hole) have been obtained.

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